CLAIMS:

1. A method of forming a lattice-tuning semiconductor substrate, comprising:

(a) defining parallel strips (12) of a Si surface by spaced parallel isolating means (2; 11);

(b) selectively growing a first SiGe layer (13) on the strips (12) such that first dislocations (14) extend preferentially across the first SiGe layer (13) between the isolating means (2; 11) to relieve the strain in the first SiGe layer (13) in directions transverse to the isolating means (2; 11); and

(c) growing a second SiGe layer (13a) on top of the first SiGe layer (13) to overgrow the isolating means (2; 11) such that second dislocations (15) form preferentially within the second SiGe layer (13a) above the isolating means (2; 11) to relieve the strain in the second SiGe layer (13a) in directions transverse to the first dislocations (14).

2. A method according to claim 1, wherein the first SiGe layer (13) has a Ge composition ratio that is substantially constant within the layer (13).

3. A method according to claim 1 or 2, wherein the second SiGe layer (13a) has a Ge composition ratio that is substantially constant within the layer (13a).

4. A method according to claim 1, 2 or 3, wherein at least one of the SiGe layers (13, 13a) has a Ge composition ratio that increases within the layer from a first level to a second level greater than the first level.

5. A method according to any preceding claim, wherein at least the first SiGe layer (13) is annealed at an elevated temperature in order to substantially fully relieve the strain in the layer (13).

6. A method according to claim 5, wherein the growth of the first and second SiGe layers (13, 13a) is carried out at a temperature in the range from room temperature to 1200°C, and preferably in the range from 350 to 900°C, and the annealing of at least the first SiGe layer (13) is carried out at an elevated temperature in the range from room temperature to 1500°C, and preferably in the range from 500 to 1200°C.

7. A method according to any one of claims 1 to 6, wherein the first and second SiGe layers (13, 13a) are formed by a single continuous growth process.

8. A method according to any one of claims 1 to 6, wherein intermediate processing is conducted between the growth of the first SiGe layer (13) and the growth of the second SiGe layer (13a).

9. A method according to claim 8, wherein the intermediate processing incorporates a step of annealing the first SiGe layer (13) at an elevated temperature in order to substantially fully relieve the strain in the first SiGe layer (13).

10. A method according to claim 8 or 9, wherein the intermediate processing step incorporates a chemo-mechanical polishing step.

11. A method according to any preceding claim, wherein the first SiGe layer (13) is grown by a selective epitaxial growth process.

12. A method according to claim 11, wherein the epitaxial growth process is chemical vapour deposition (CVD).

13. A method according to claim 11, wherein the epitaxial growth process is molecular beam epitaxy (MBE).

14. A method according to any preceding claim, wherein the strips of Si oxide have a thickness in the range of 10 nm to 1000 nm, and preferably in the range from 400 nm to 700 nm.

15. A method according to any preceding claim, wherein the strips (12) of Si oxide have a width in the range from 100 nm to 10 μm, and preferably about 1 μm.

16. A method according to any preceding claim, wherein the strips (12) of Si oxide are spaced apart by a distance in the range from 100 nm to 100 μm, and preferably in the range from 5 μm to 20 μm.

17. A method according to any preceding claim, further comprising the step of growing on top of the first and second SiGe layers (13, 13a) a strained Si layer within which one or more semiconductor devices are formed.

18. A method according to any one of claims 1 to 17, wherein the isolating means comprises spaced parallel walls (2; 11) of Si oxide on the Si surface.

19. A method according to one of claims 1 to 17, wherein the isolating means comprises spaced parallel trenches in the Si surface.

20. A method according to one of claims 1 to 17, wherein the isolating means comprises spaced parallel walls of Si nitride on the Si surface.

21. A lattice-tuning semiconductor substrate formed by a method according to any preceding claim.